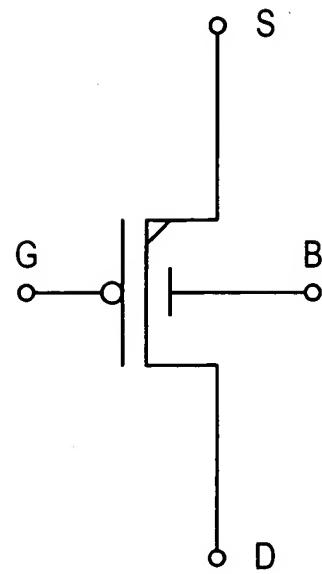
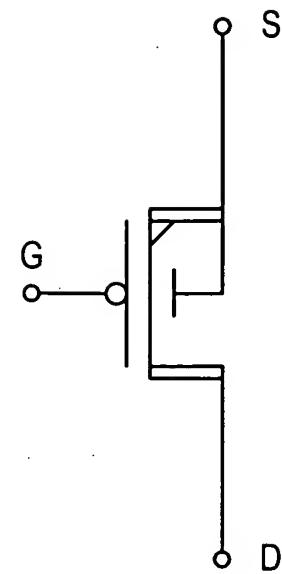


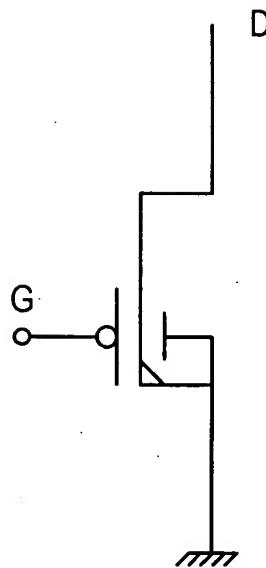
(a) 5V NMOS



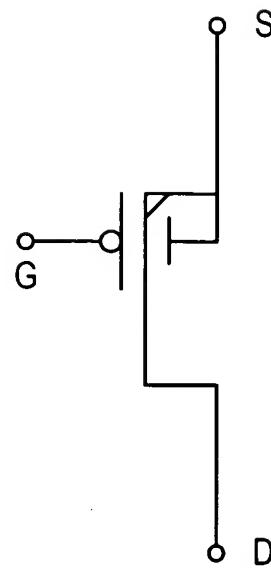
(b) 5V PMOS



(c) HV PMOS



(d) HV NDMOS



(e) HV PDMOS

PRIOR ART

FIG. 1

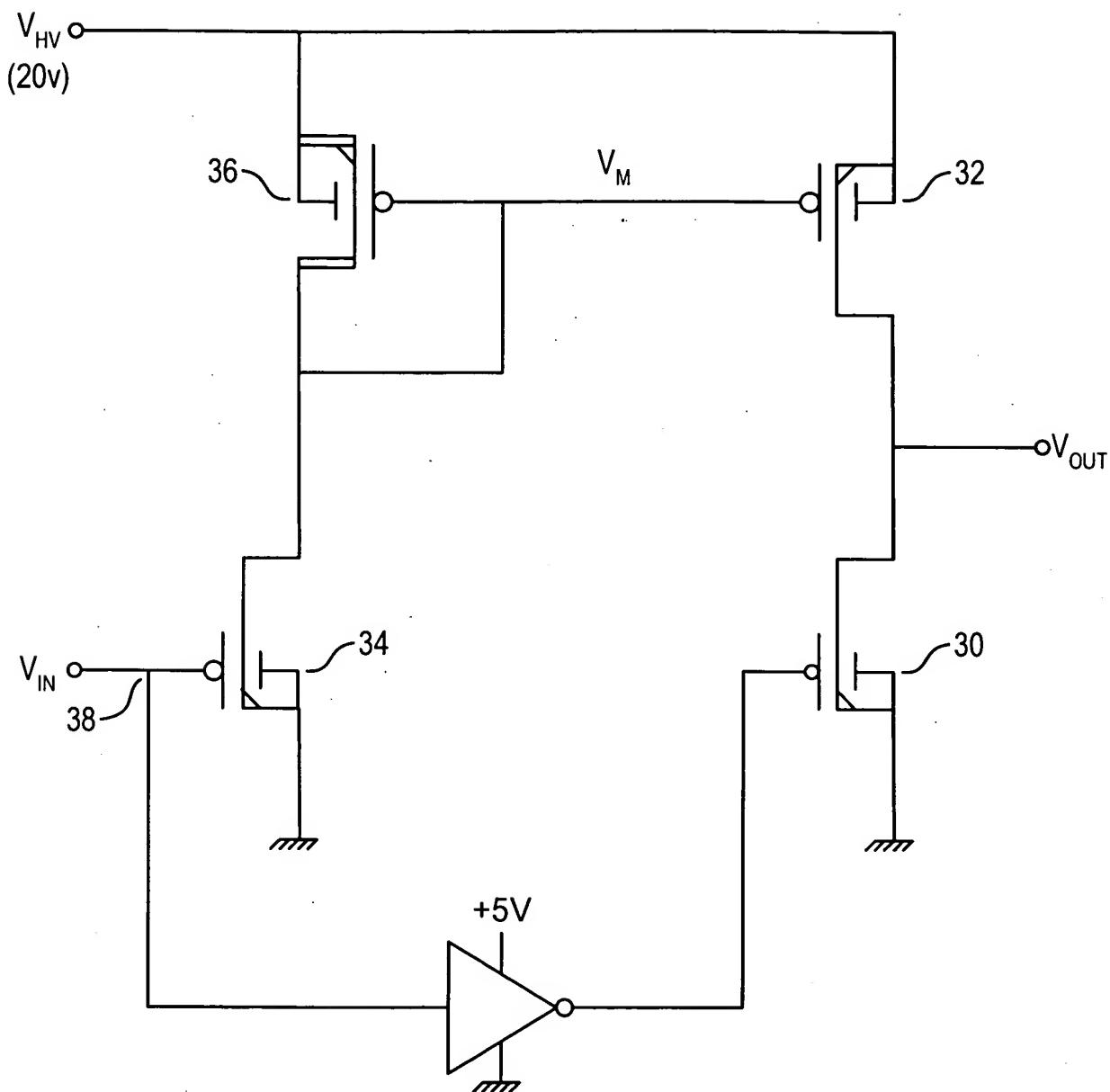
PRIOR ART

FIG. 2

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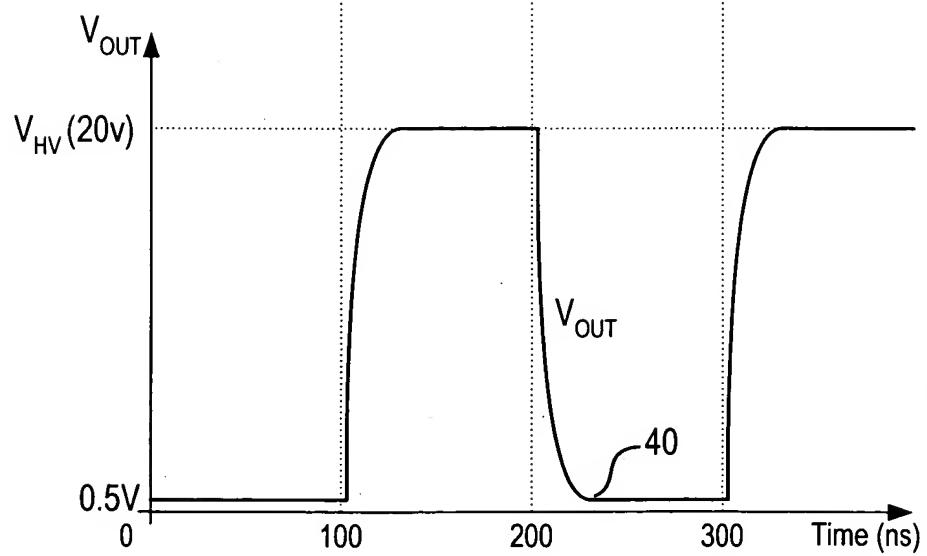
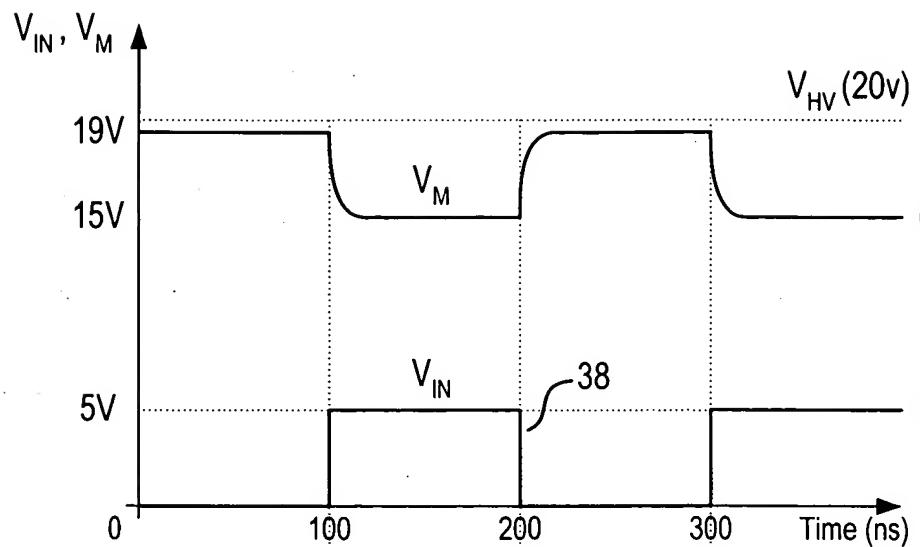
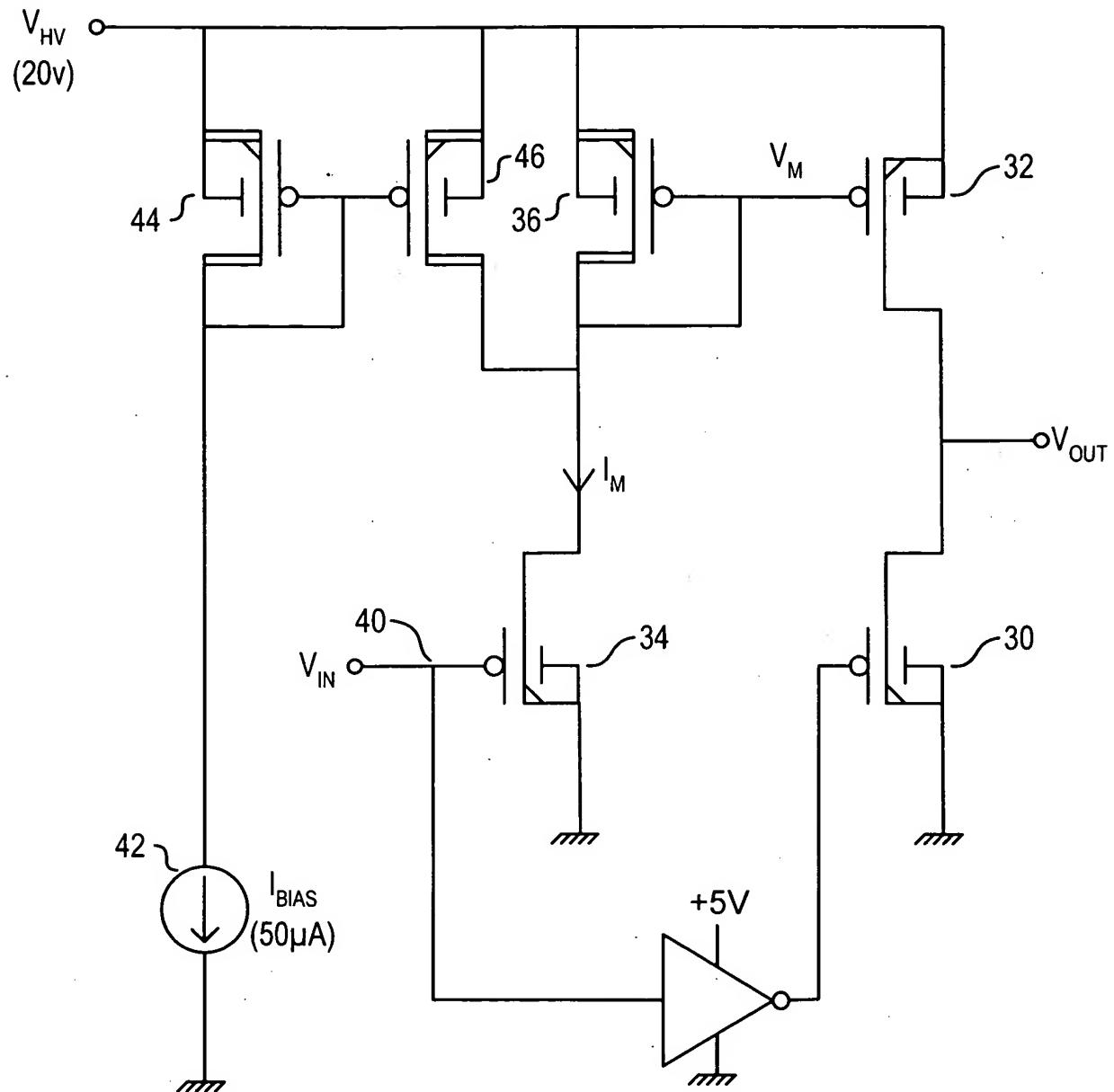


FIG. 3C

PRIOR ART

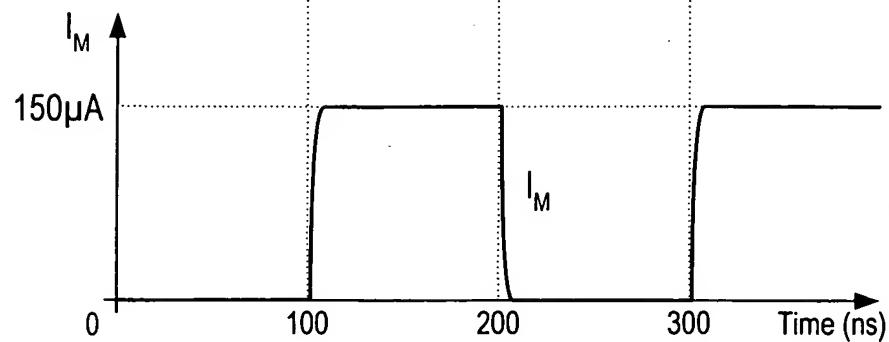
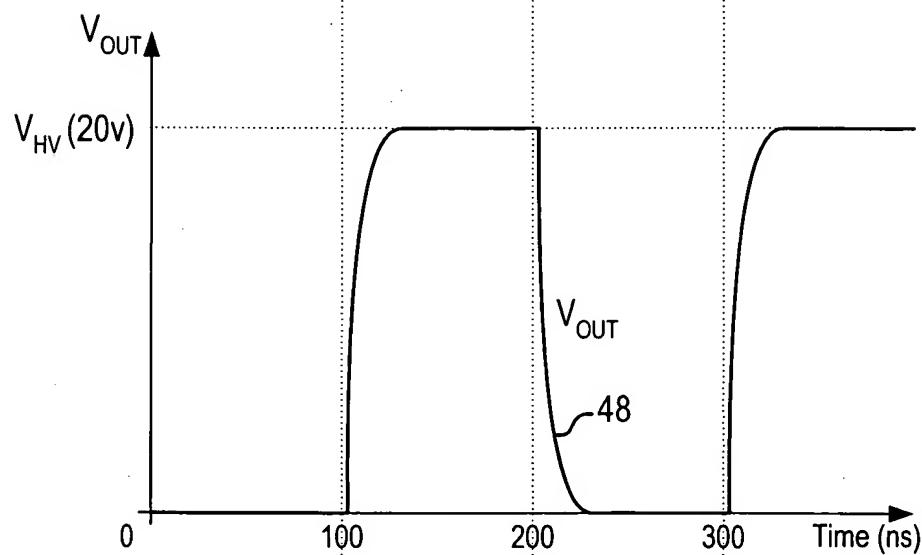
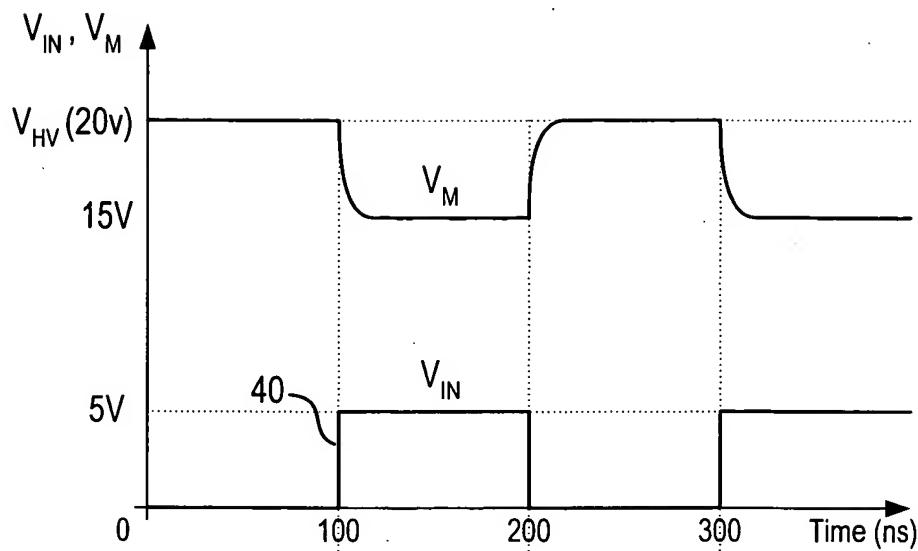
(4/25)



PRIOR ART

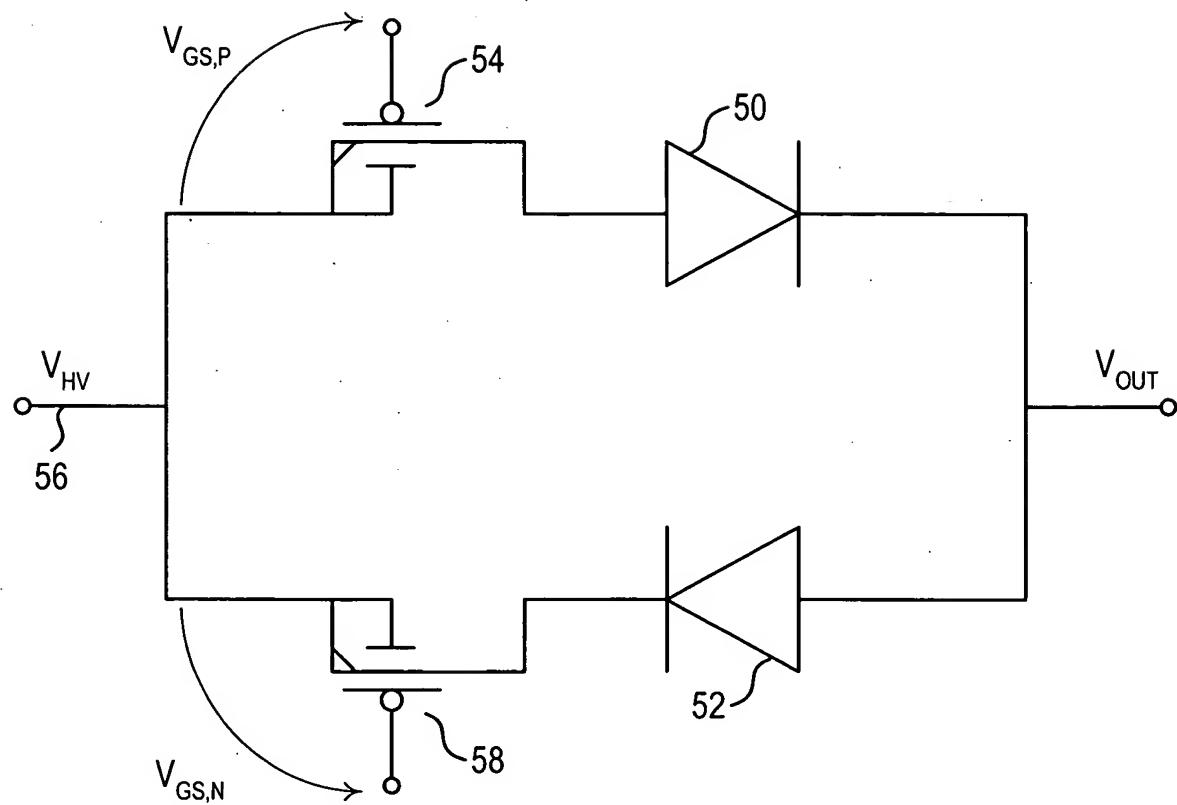
*FIG. 4*

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PRIOR ART

(6/25)



PRIOR ART

*FIG. 6*

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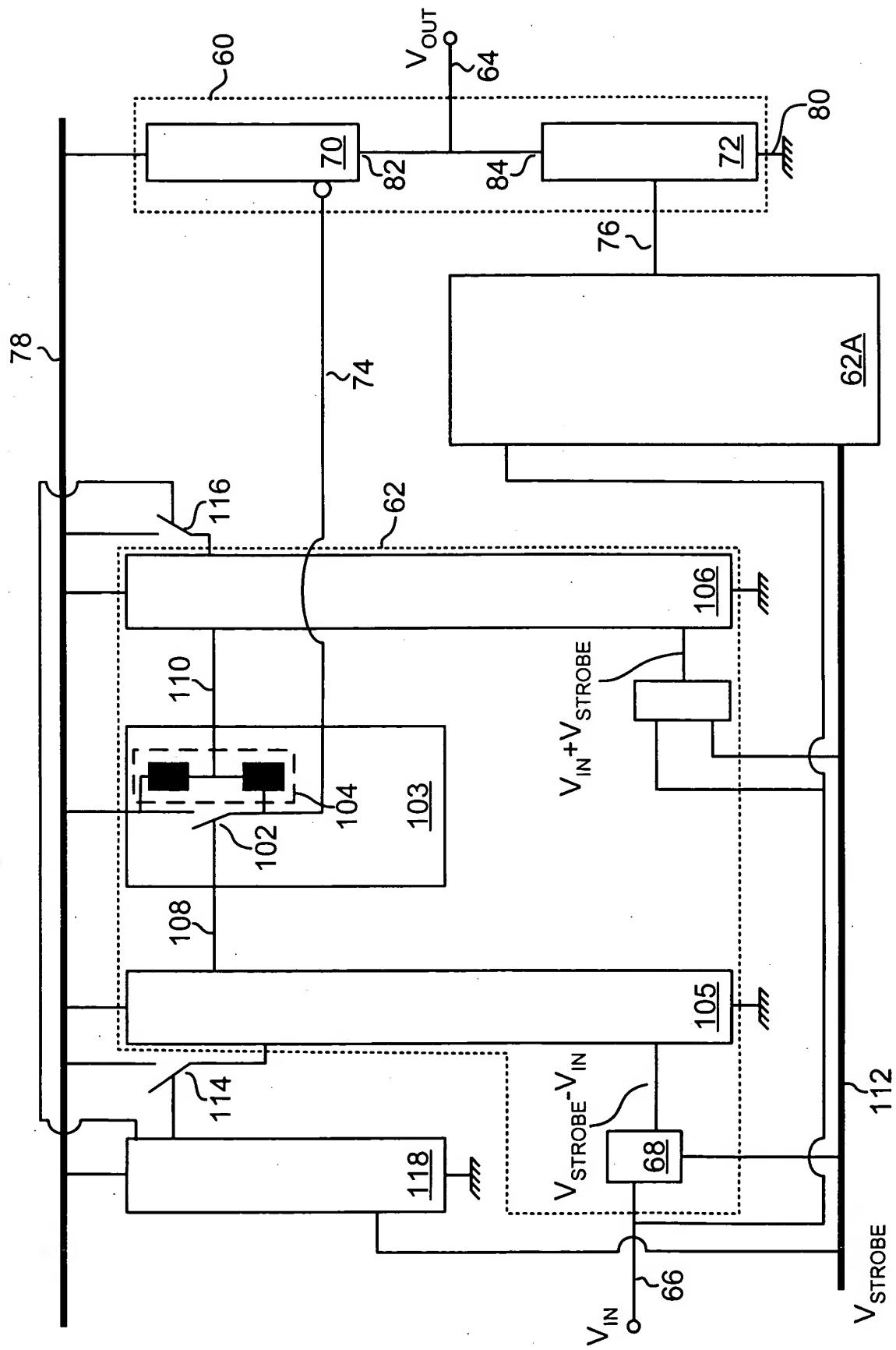


FIG. 7

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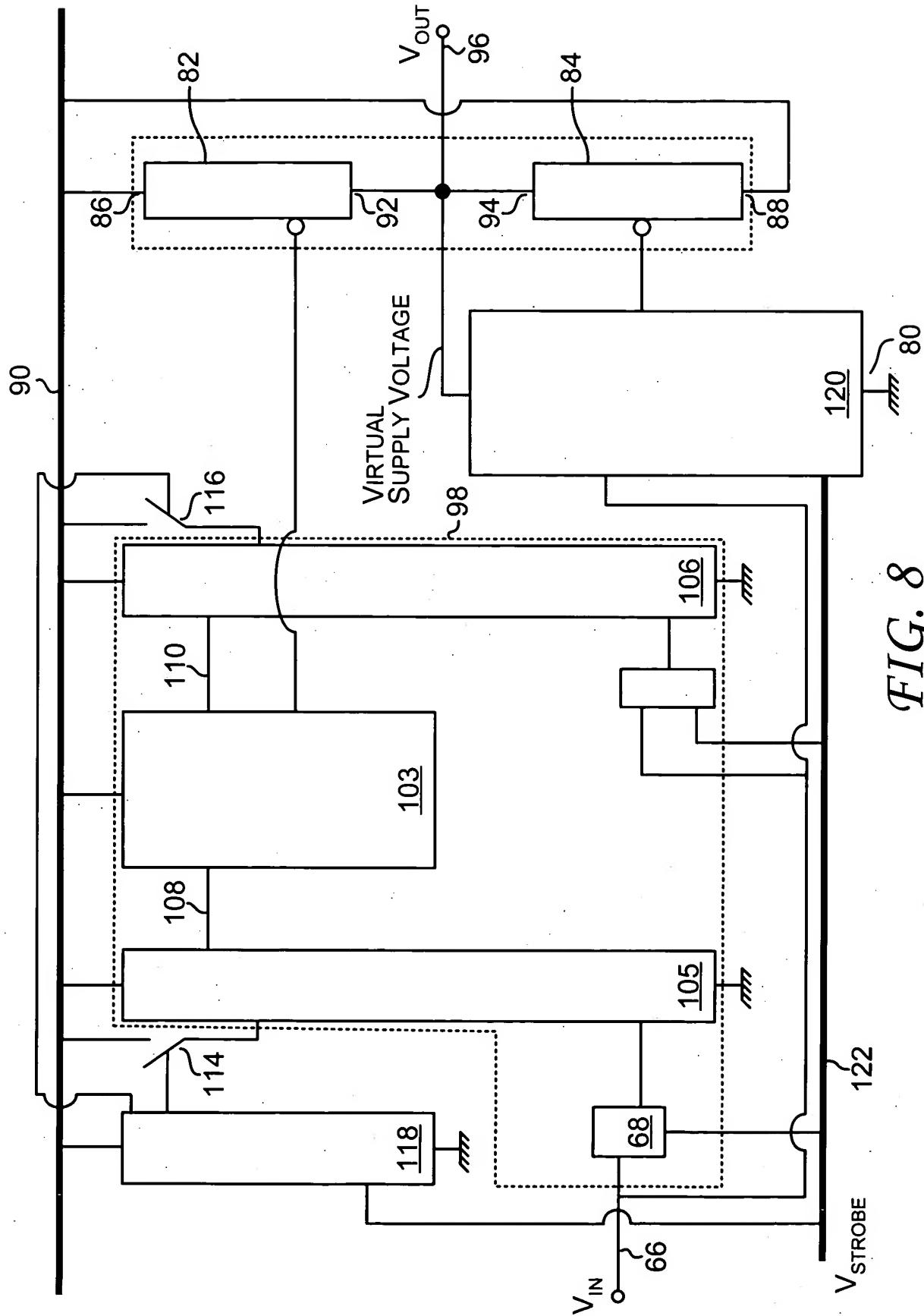


FIG. 8

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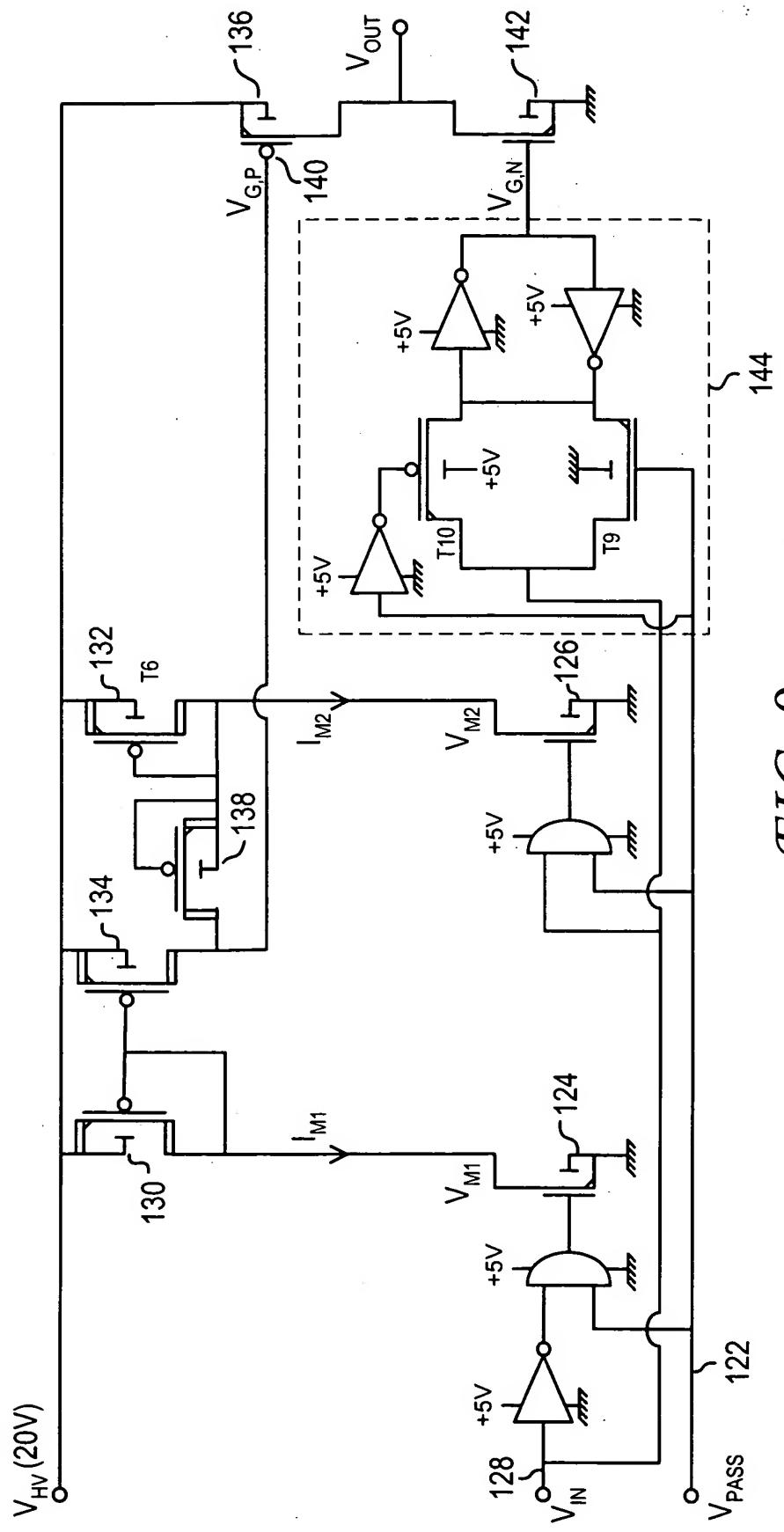


FIG. 9

(10/25)

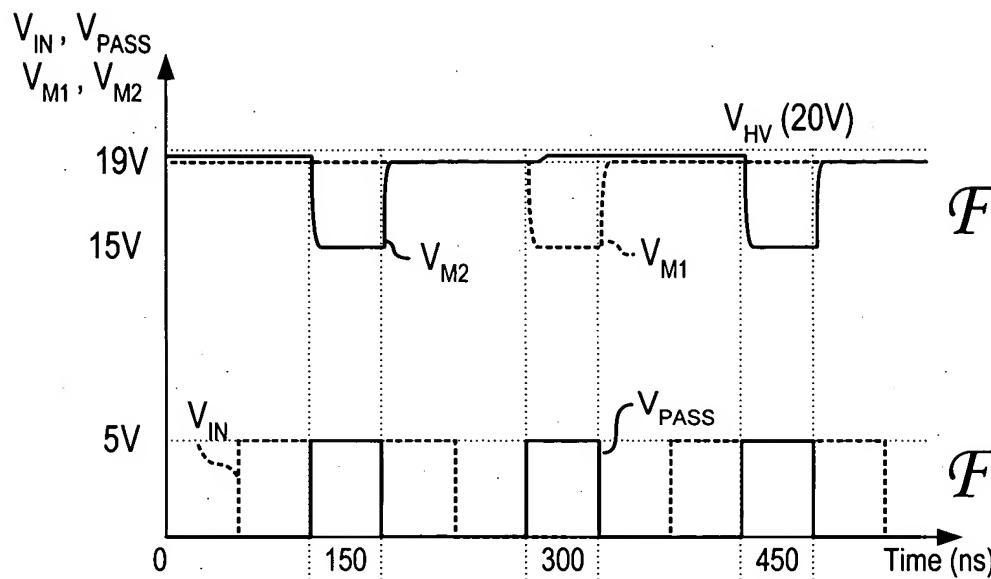
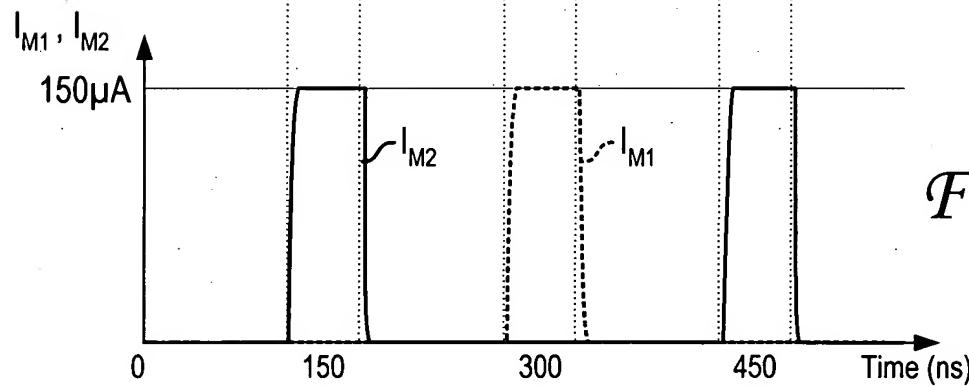
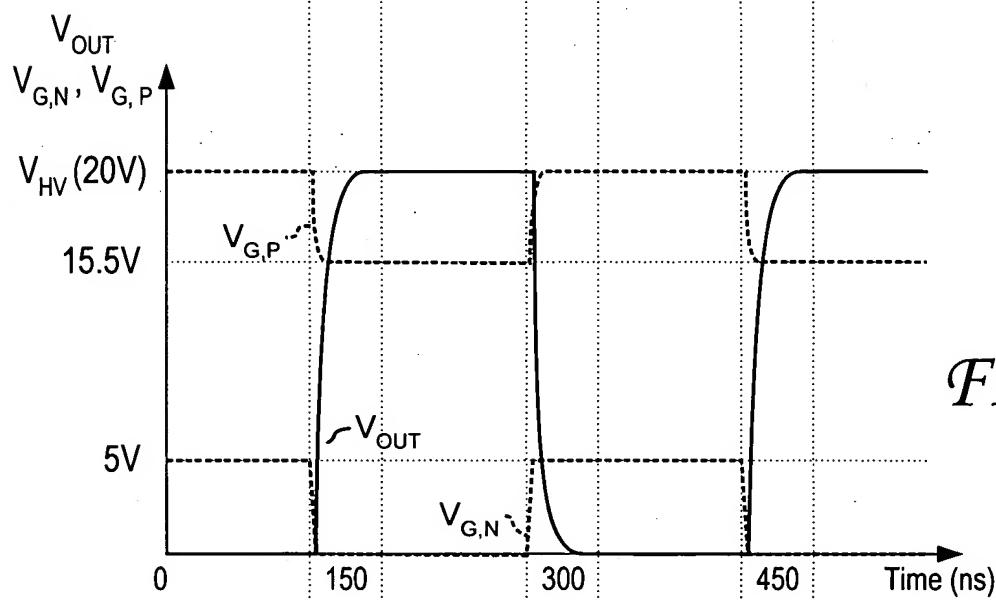


FIG. 10D



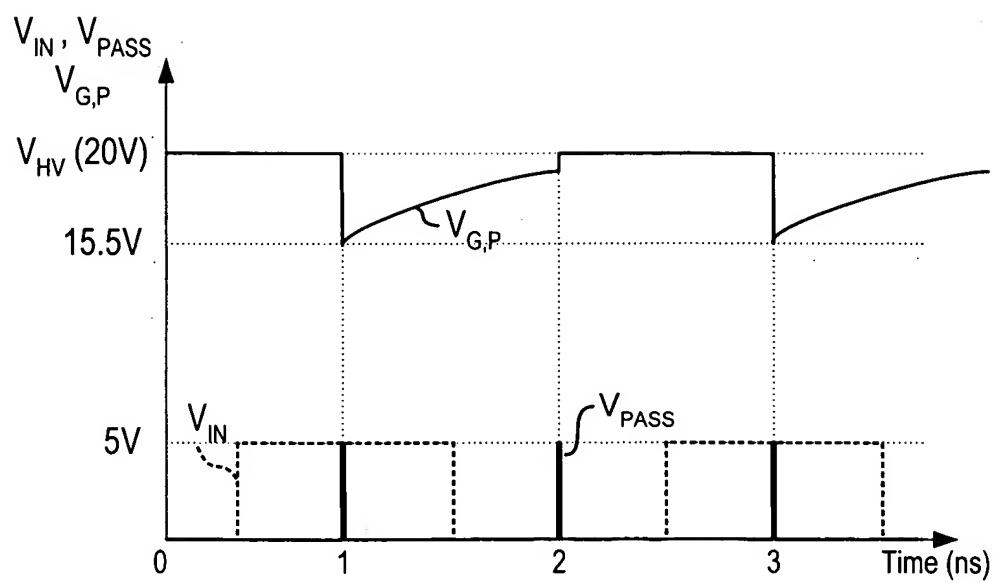
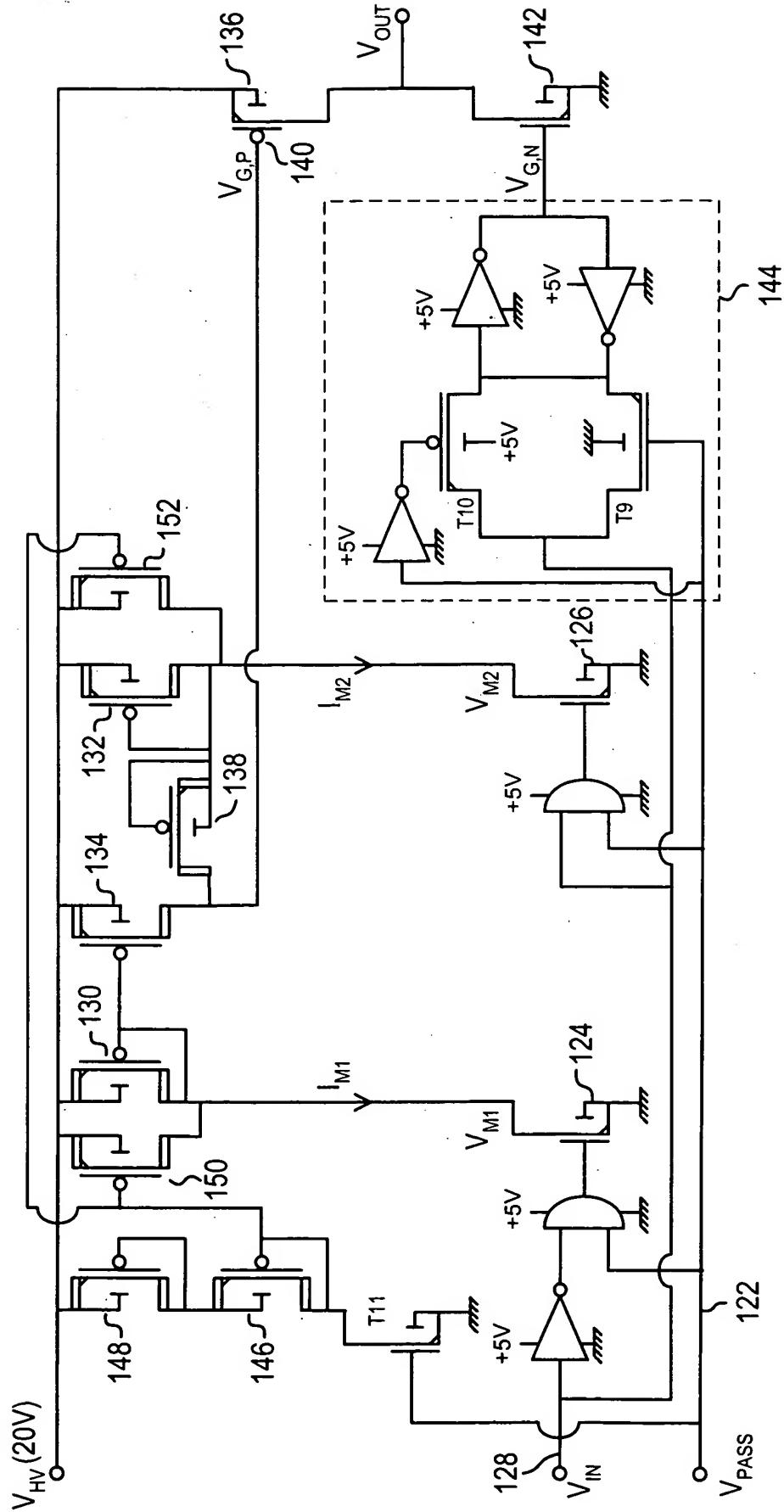


FIG. 11

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IMPROVED DYNAMICALLY CONTROLLED HIGH-VOLTAGE LEVEL-SHIFTER WITH EXTREMELY LOW POWER CONSUMPTION

FIG. 12

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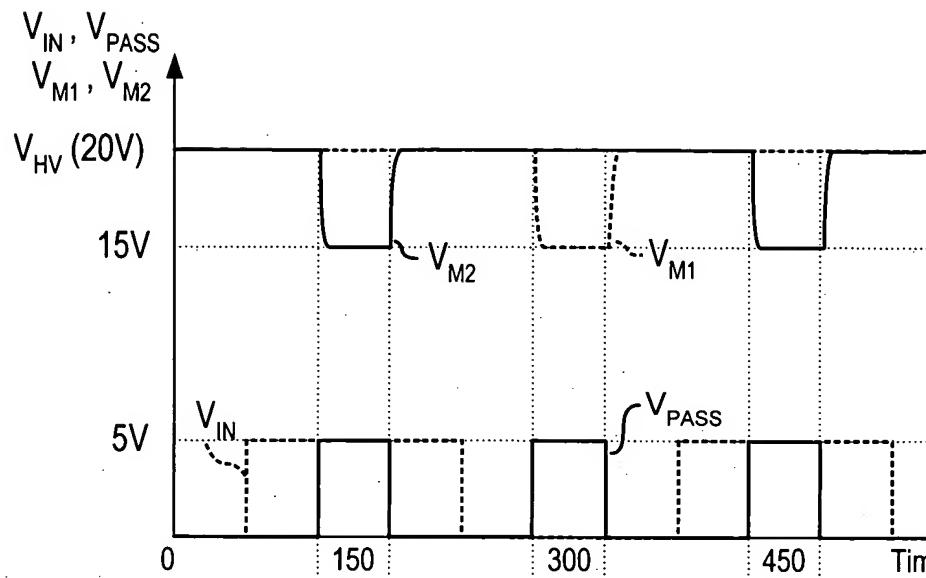
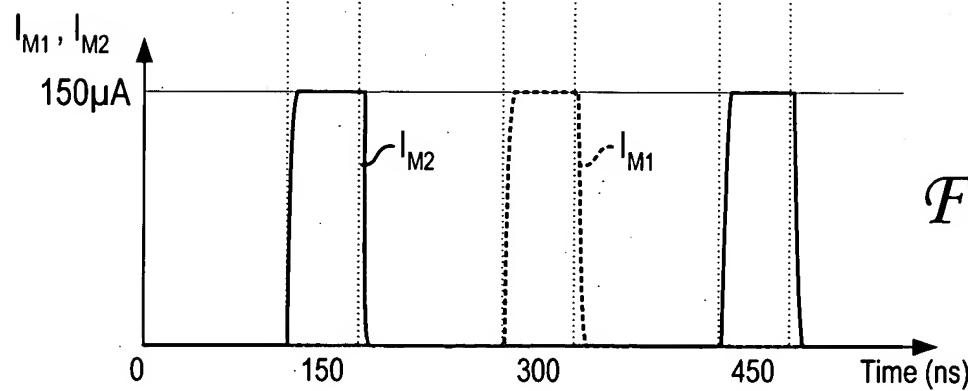
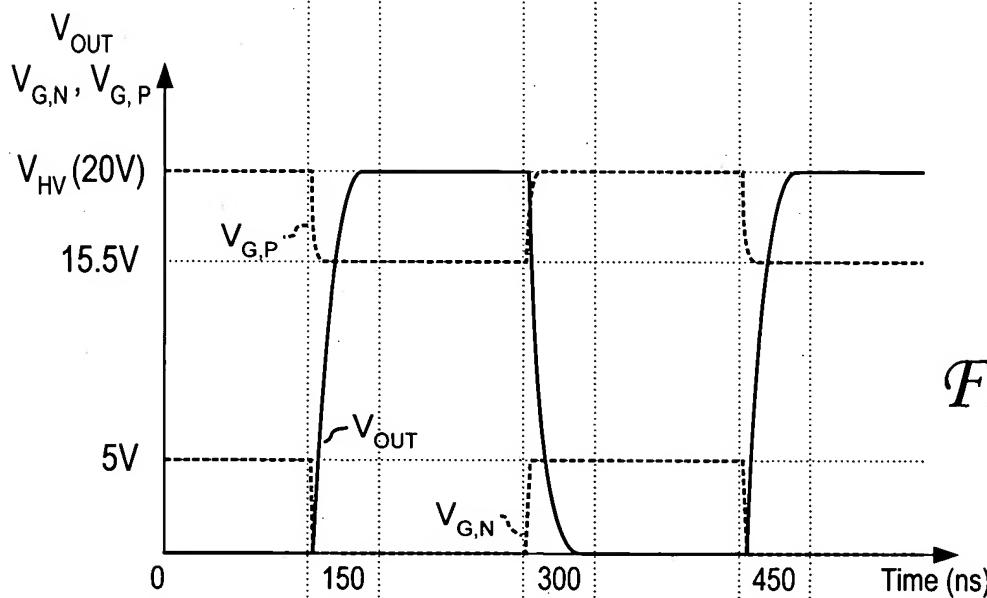


FIG. 13C



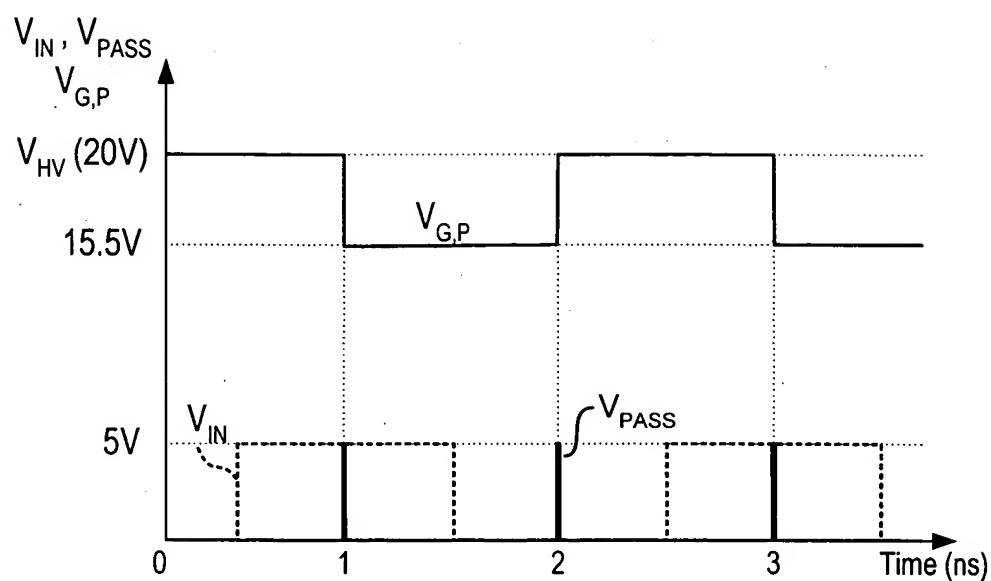


FIG. 14

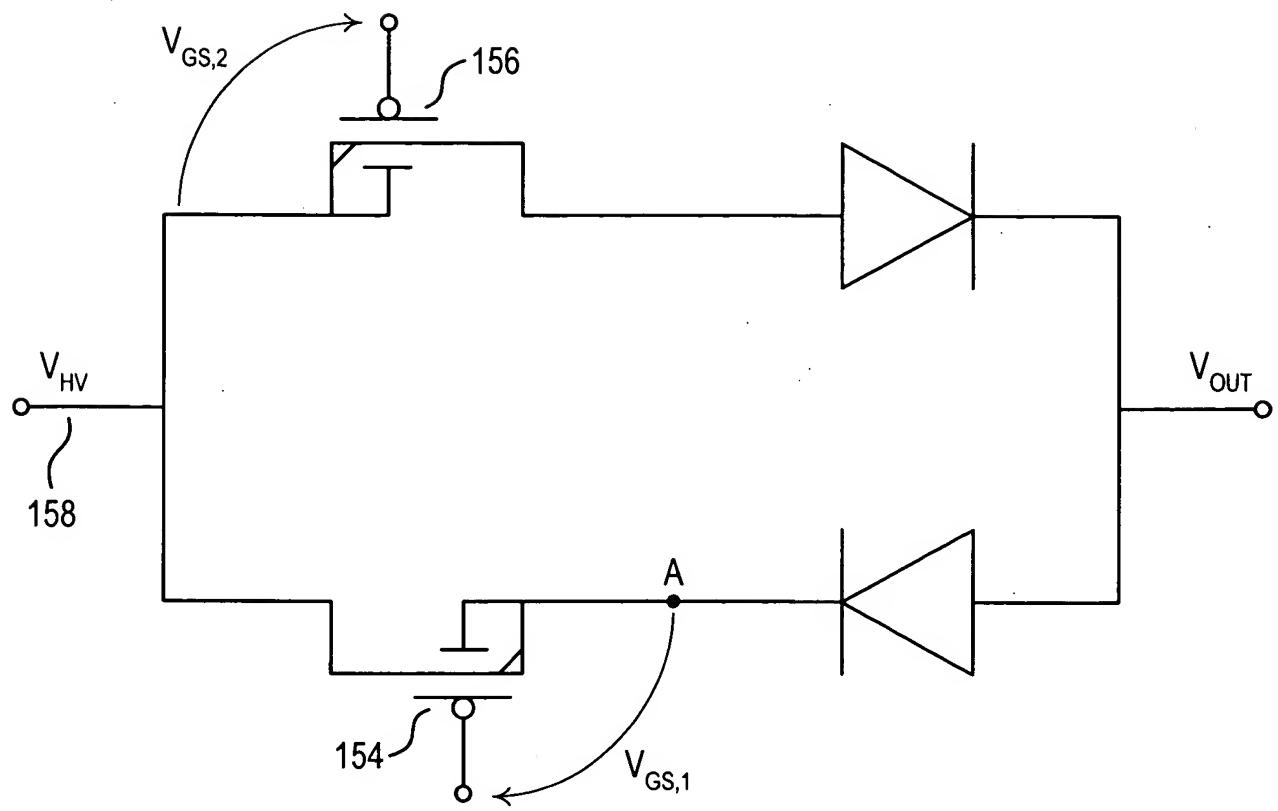
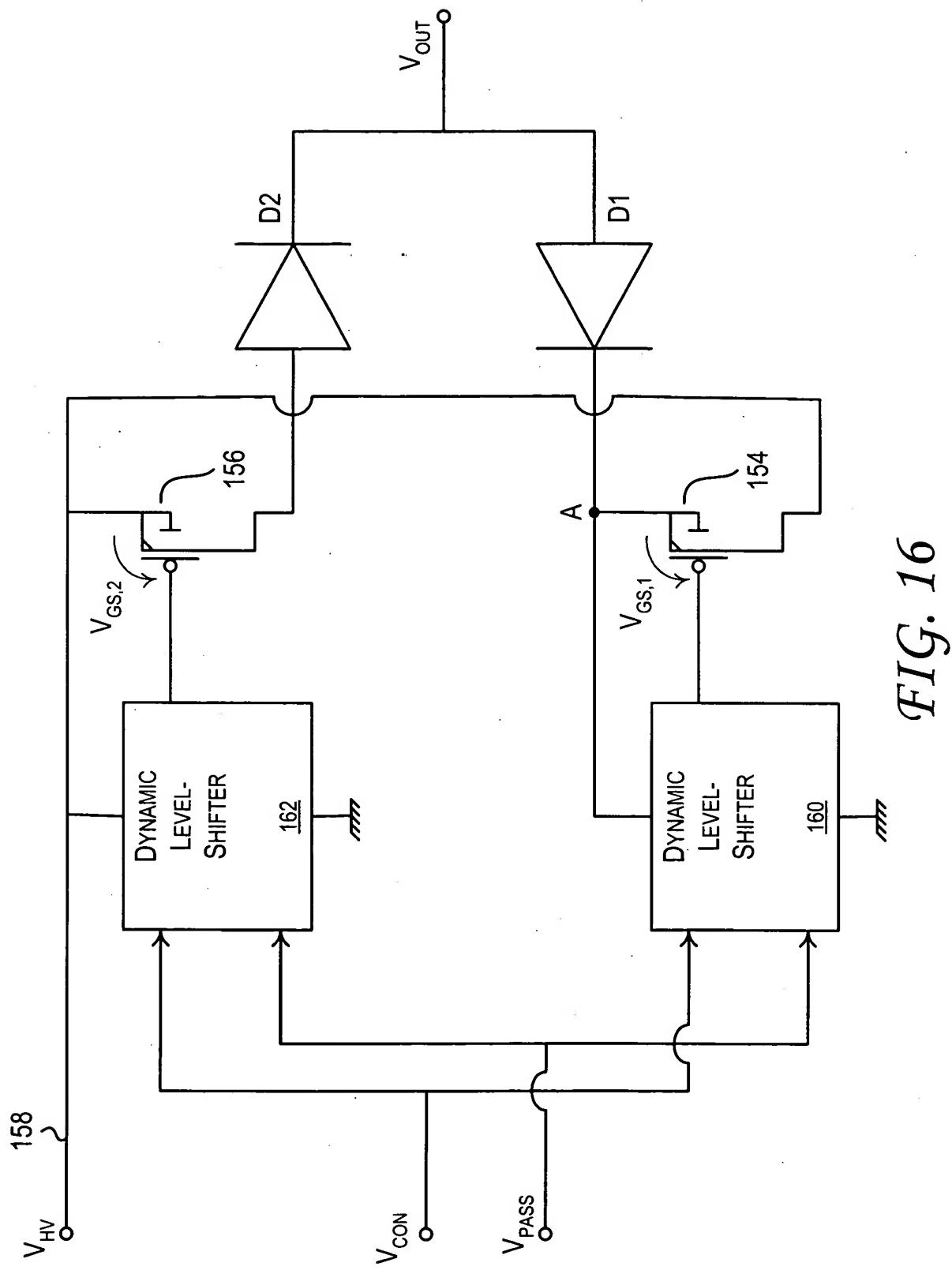


FIG. 15

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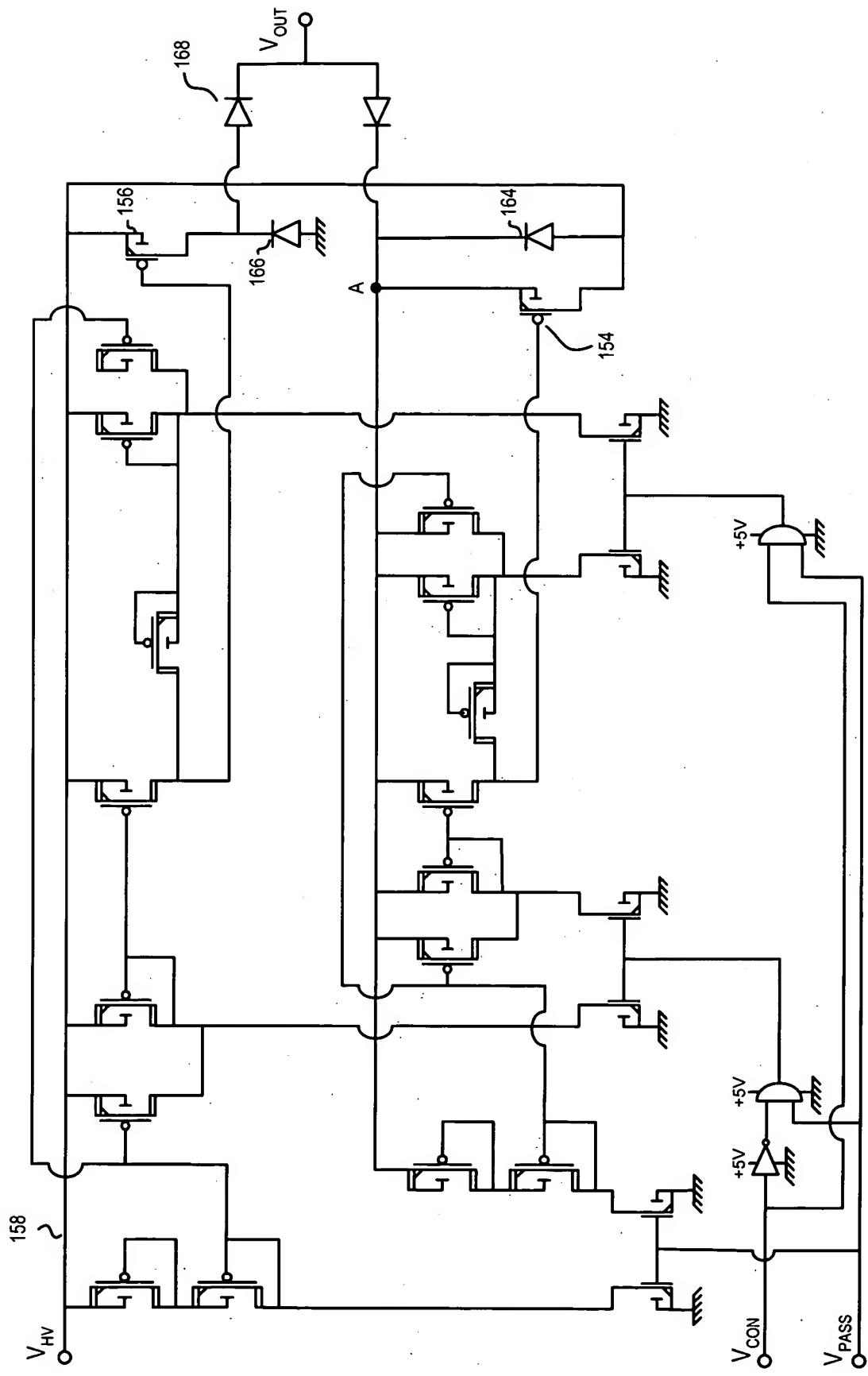


FIG. 17

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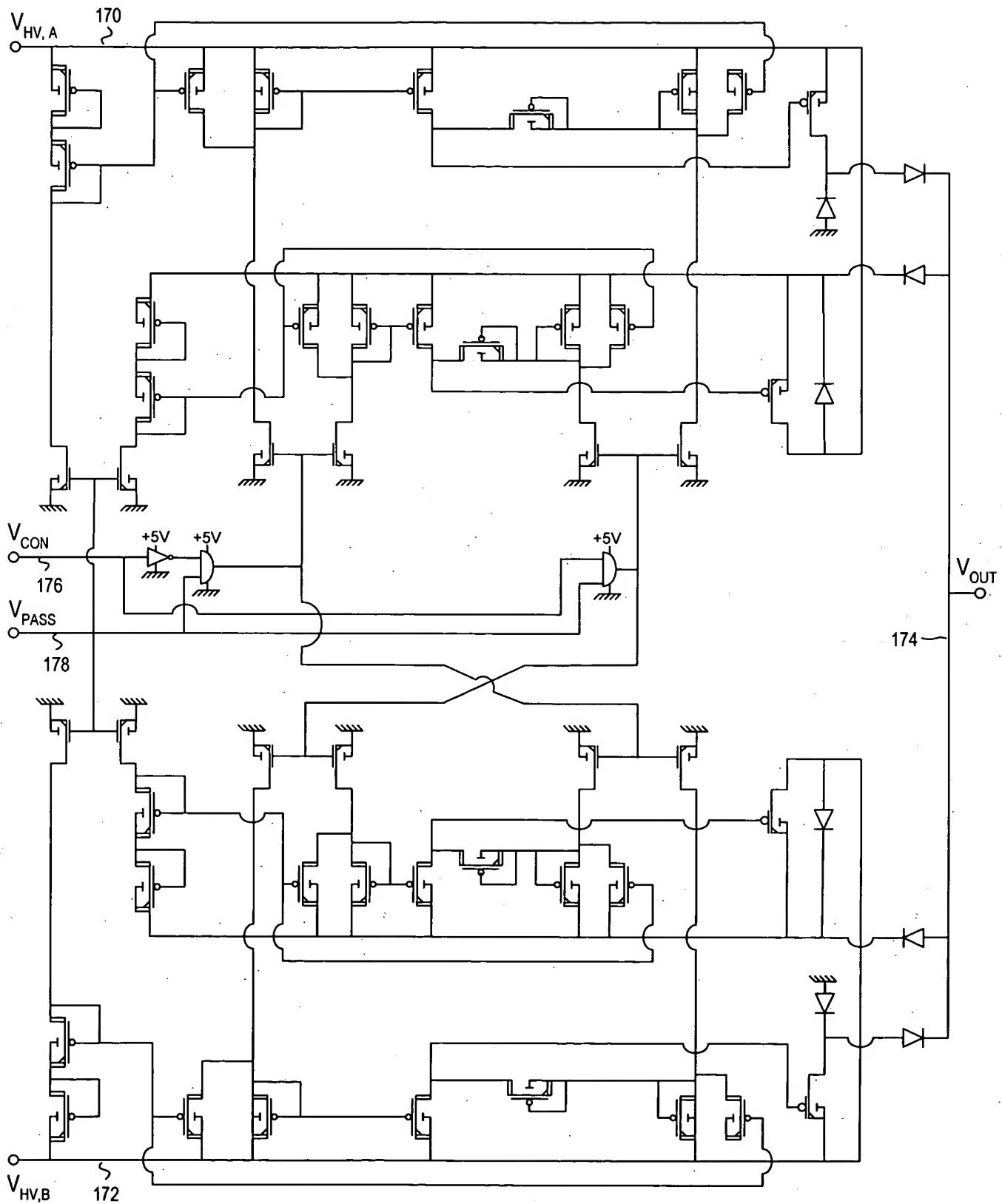


FIG. 18

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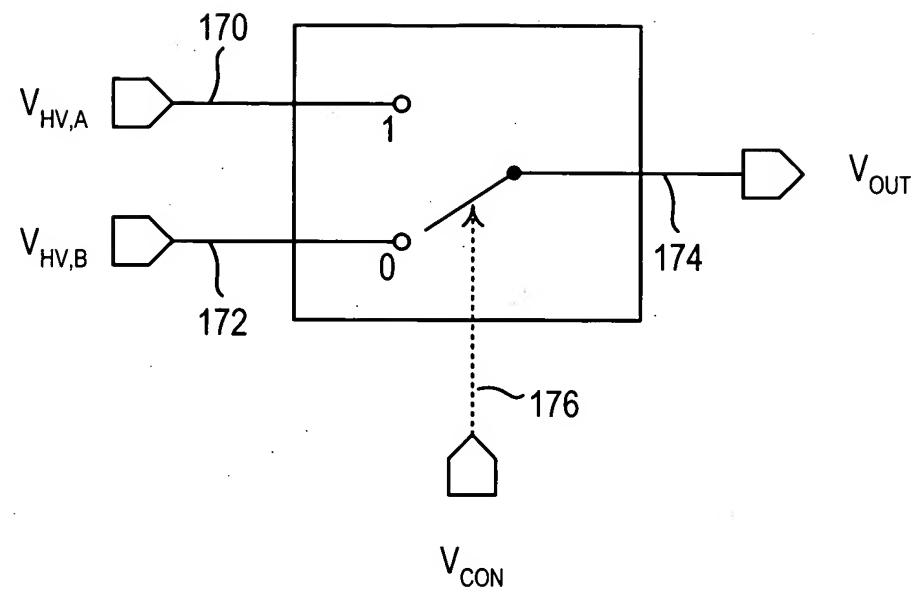


FIG. 19

(20/25)

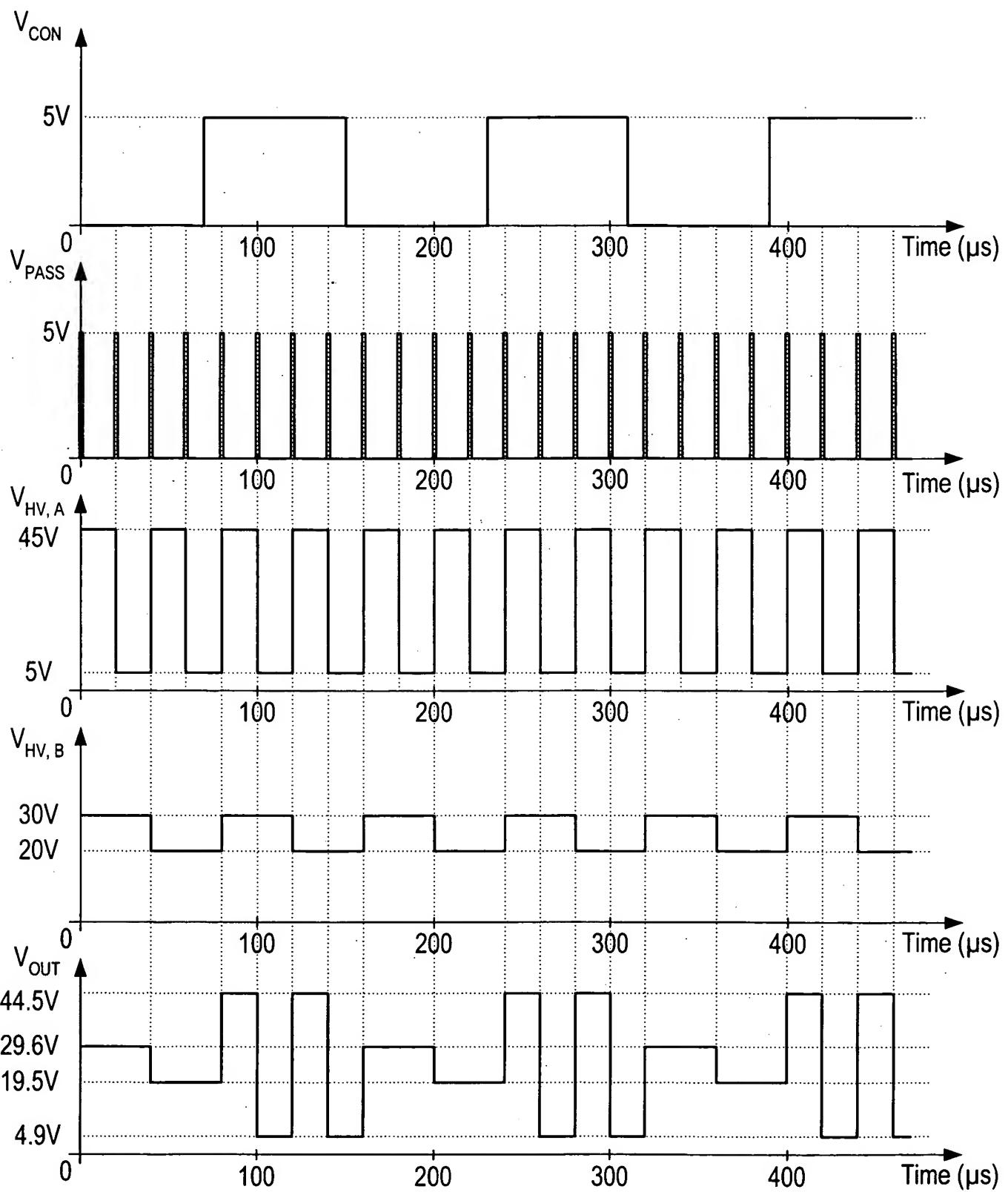


FIG. 20

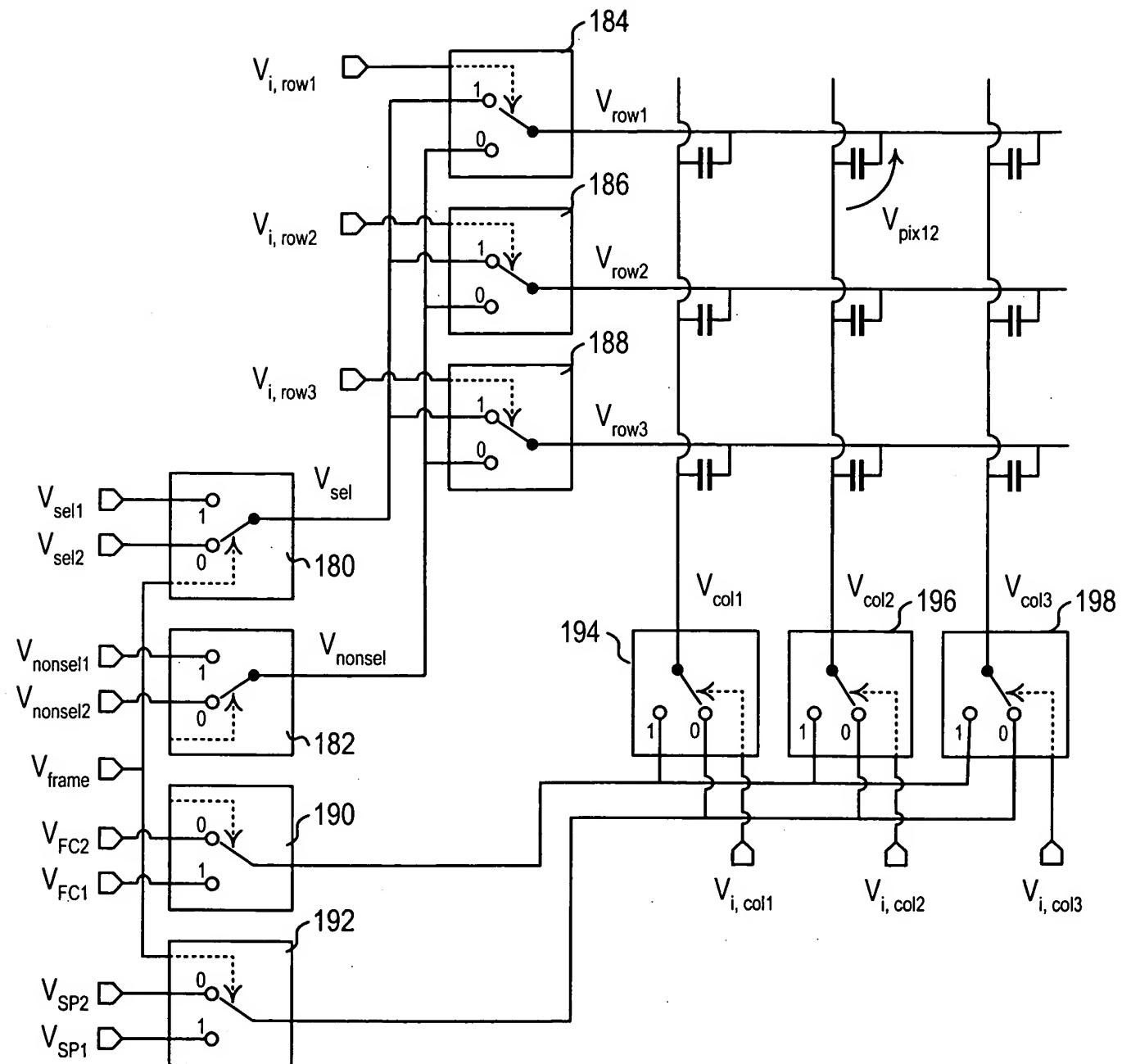


FIG. 21

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FC	SP	SP
SP	FC	FC
FC	SP	FC

*FIG. 22*

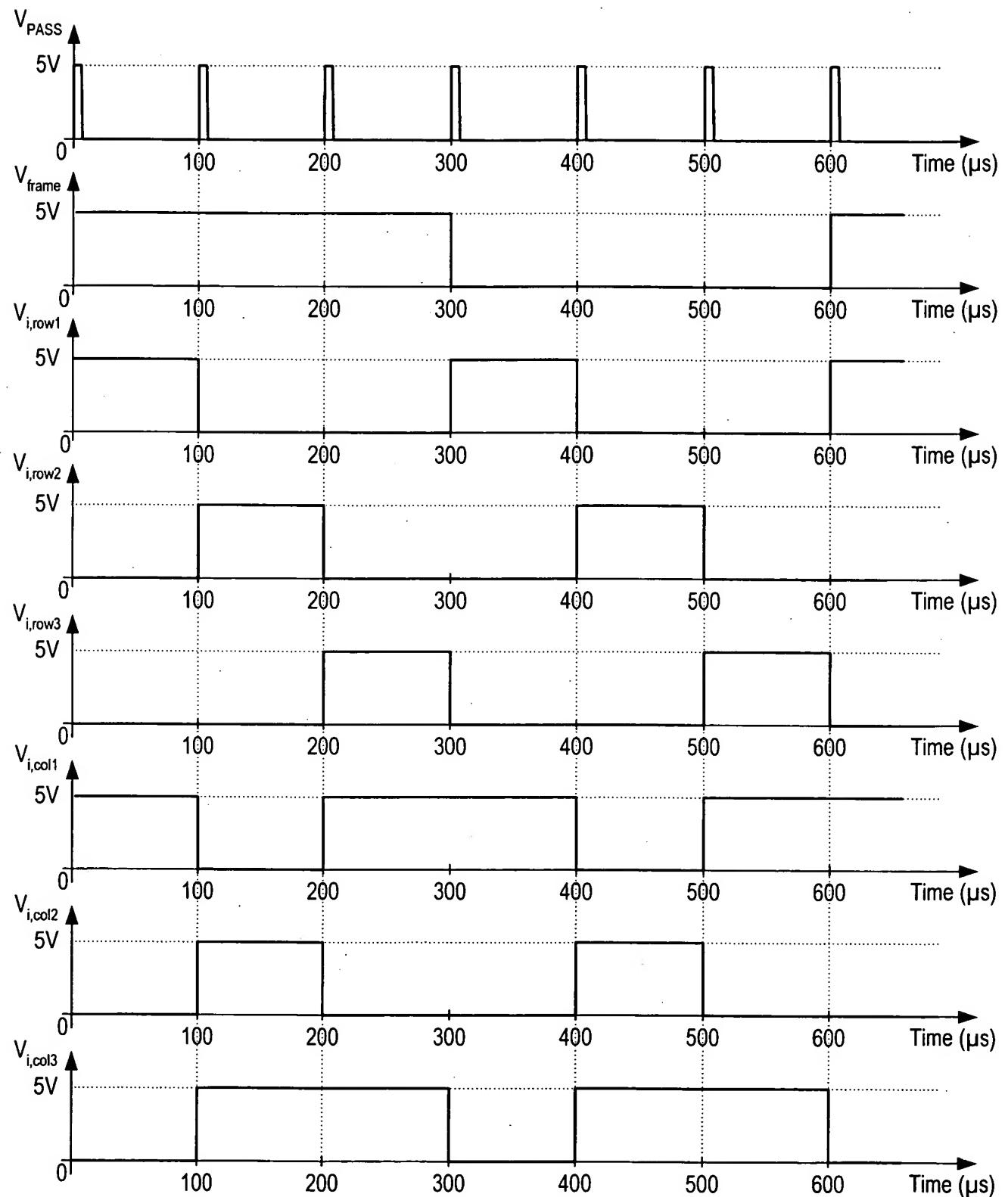


FIG. 23A

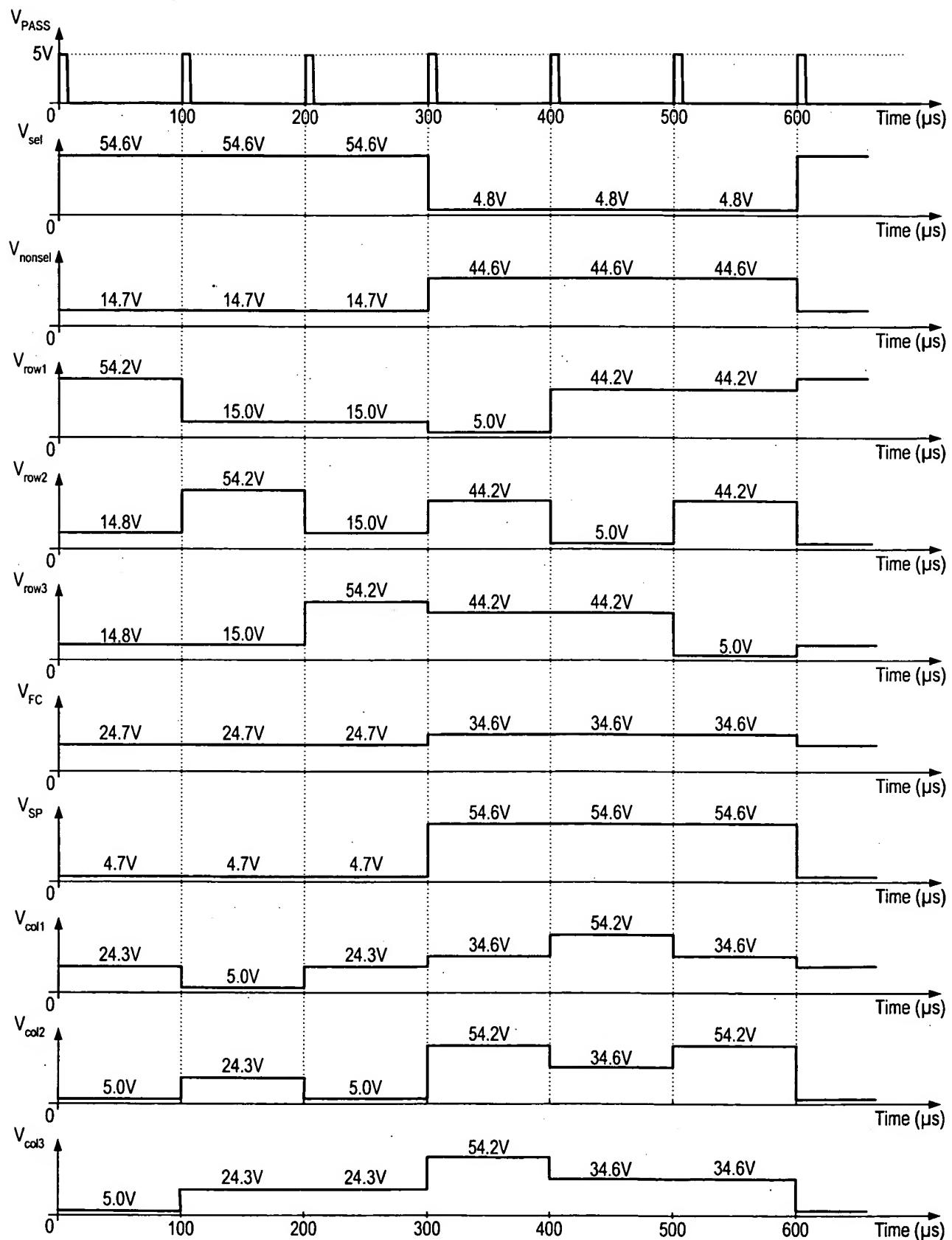


FIG. 23B

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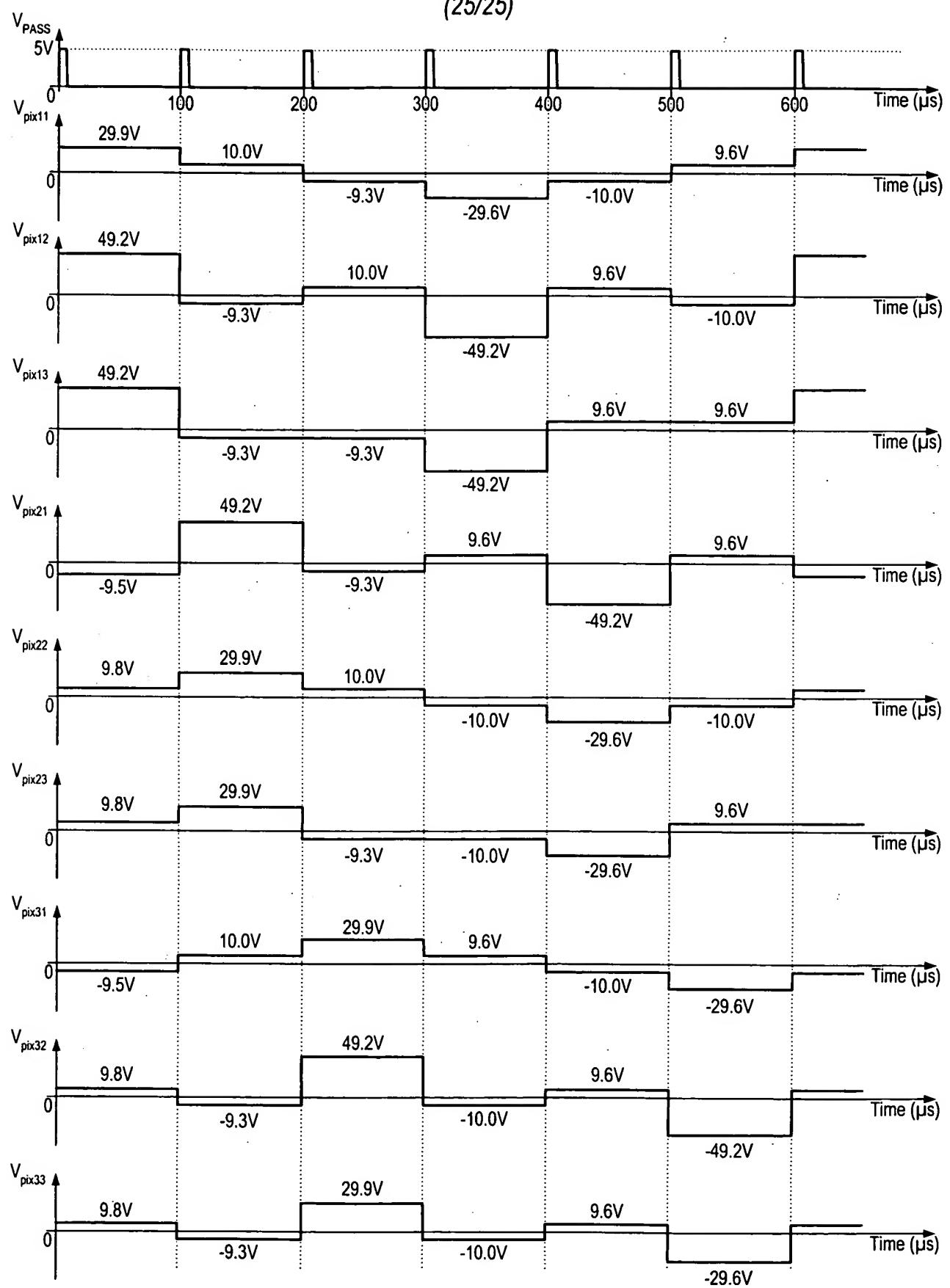


FIG. 23C